Description of **FR2804793**

The continuation of the realization of the integrated circuit comprises for example a deposit in conformity of an oxide coating TEOS 31 on layer 30, in order to find itself in a configuration similar to that of figure 1. One could also deposit a doped dielectric material with the phosphorus possibly covered with a dielectric material un-doped, for example of the TEOS. One will then possibly procedure with a flattening of this layer 1, in order to be able to carry out on his upper surface the first level of metallization which will be then supplemented in a traditional way by higher levels of metallization, mutually inter-connected by vias. It is however advisable to note here that this flattening is not essential if the relief obtained is weak and compatible with the traditional later stages of manufacture of the integrated circuit.

Integrated circuits comprising of transistors CMOS (transistors complementary to field effect to insulated grid) are manufactured today with polycrystalline silicon grids which are a material having thermal and mechanical properties close to those of the silicon substrate. This polycrystalline silicon is in general transformed a silicide of metal into surface, by deposit of metal (for example titanium) and reaction with silicon at the places where polycrystalline silicon (polysilicon) emerges. This metal silicide has the advantage of conferring equipotential metal on the dual grids used in current technologies CMOS. Silicidization also has the advantage of reducing resistances of the lines of polysilicon used for the grids of the transistors, and makes it possible to use in certain cases these lines like lines of local interconnection.

However, the metal silicide used today is made of way car-row (i.e. simultaneously) at the same time on the lines of polysilicon of the grids and on the areas of source and drain of the transistors. This improves the contact on the areas of source and drain and contributes to reduce the resistance of access to the channel of the transistor in very short transistors MOS and to very fine junction. On the other hand, this presents the disadvantage of having to form a metal silicide having a thickness compatible with the thickness of the junctions source/substrate and drain/substrate, to avoid their drilling. However, since the junctions are increasingly fine for the leading-edge technologies, the metal silicide currently strongly thinned on the areas of source and drain, but also consequently on the areas of grids in polysilicon. Consequence, the resistance of the lines of "siliciuré" polysilicon thus tends to increase for rising generation of transistors since the thickness of the layer of metal silicide is finer.

And, this is particularly awkward for analogical applications functioning in the field of the high frequencies especially in the field of the radio frequencies, where the frequencies exceed gigahertz.

The invention aims at bringing a solution to this problem.

A goal of the invention is to adjust the value of resistance of grid of a transistor while avoiding a drilling of the junctions drain/substrate and source/substrate.

The invention thus proposes a process of adjustment of the value the resistance of grid of a transistor of an integrated circuit carried out within substrate semiconductor and covered with an insulating layer typically of the silicon nitride surmounted by another oxide such as silicon tetraorthosilicate (TEOS in English language).

The process comprises a stage in which one discovers polysilicon of the initial grid of the transistor which is surrounded by insulating spacers, a stage in which one forms on the initial grid thus discovered an extension of grid by depositing by selective epitaxy a layer of polysilicon having a selected thickness. The process also comprises a stage in which one carries out a silicidization of at least a part of the extension of grid on a thickness chosen, way to obtain a final grid for the transistor formed of the initial grid surrounded by the spacers and surmounted extension by grid thus siliciurée.

The invention is thus remarkable in this direction in particular silicidization will consume at least a part of silicon deposited and forming the extension of grid, without affecting the

junctions source/substrate and drain/substrate. This silicidization could advantageously be done at low temperature and the thicknesses of epitaxial polysilicon and metal silicide could be adjusted to reach the values of resistance required by the application concerned.

According to the thickness chosen for epitaxial polysilicon, this one will be able to extend laterally at a distance proportional to the thickness, taking into account the amorphous polycrystalline character of silicon being used as germ, i.e. the silicon of the initial grid. In other words, one can make overflow the extension of grid laterally compared to the initial grid, which makes it possible to obtain a grid forms "T of them". This has the advantage, in certain applications, to be able to preserve the same volume of polysilicon for the extension of grid all reducing the height of the extension of grid and by compensating for this reduction height by a side overflow. This has the advantage of reducing the relief created by the epitaxy.

In addition, although it is in theory possible to carry out a silicidization only on one part of the extension of grid, for example at the top, by carrying out for example a selective deposit metal, it can prove preferable, in certain applications, to carry out a silicidization of the totality of the extension of grid, which in particular results in carrying out a silicidization of the sides of the extension of grid. It is thus possible to distribute the desired quantity of metal silicide taking into account the value of resistance wished, on the totality of the extension of grid, which consequently results in having a lower thickness.

This silicidization of the totality of the extension of grid, in combination with an extension of polysilicon grid overflowing laterally compared to the initial grid, makes it possible to adjust and decrease value of the resistance of grid while avoiding too important heights for the final grid.

When the integrated circuit comprises moreover complementary transistors, i.e. transistors NMOS and PMOS, one advantageously carries out each stage of the process simultaneously for all the transistors of the integrated circuit.

The invention also has as an aim an integrated circuit, comprising at least a transistor produced within a conducting semi substrate and comprising a siliciurée grid. According to a general characteristic of the invention, the grid is made of a lower part surrounded by insulating spacers and of an extension of grid overcoming the lower part and covered at least partially with a layer of a metal silicide.

According to a mode of realization of the invention, the extension of grid covered with the layer of metal silicide is broader than the lower part of the grid.

The extension of grid can be completely covered with the silicide layer of metal.

When the integrated circuit comprises moreover complementary transistors, the grids of all the transistors are, according to the mode of realization, respectively formed of a lower part surrounded by insulating spacers and of an extension of grid overcoming the lower part and covered with a layer of a metal silicide.

Other advantages and characteristic of the invention will appear with the examination of the detailed description of modes of implementation and realization, by no means restrictive, and of the annexed drawings, on which figures 1 to 5 very schematically illustrate mode of implementation of the process according to the invention, figure 5 schematically illustrating a mode of realization of a transistor according to the invention.

Figure 1, reference 4 indicates, conducting semi substrate, for example out of silicon of the type P, in which one carries out a comprising integrated circuit of the transistors complementary to field effect to isolated grid. On figure 1, one A represents only two transistors, namely a transistor TI (for example a transistor NMOS) and a transistor T100 (for example a transistor PMOS).

Transistors T1 and T100 are insulated by an insulating area 6, for example of the type distinct not very deep (STI: Shallow Trench Insulation English language).

In addition, the specialist of the profession knows that, then transistors NMOS can be produced directly within substrate 4, transistors PMOS are then produced within a box 5 doped N.

Put aside the zone of side insulation 6 and box 5, the right-hand side parts and left of each figure 4 and 5 are identical. Also, the elements of the left parts of these figures, i.e. located on the left zone of side insulation 6, and which are similar or have functions similar to the elements illustrated on the right part of each one of these figures, have references increased by 100 compared to the references of these same elements illustrated on the right part. With ends of simplification, one will describe hereafter the mode of implementation and realization of the invention while referring mainly to the straight lines part of each figure.

Transistor NMOS T1 comprises in a traditional way of the established zones of source and of drain, respectively referred S and DI. In the case of a transistor NMOS, these zones S 1 and D 1 are doped N+, while the equivalent zones S 101 and D 101 of transistor PMOS T 10 1 are doped P+.

Transistor NMOS T1 comprises in addition an initial grid G1 polysilicon, resting on substrate 4 by the intermediary of an oxide OX 1. In addition, this grid is surrounded classically by insulating areas, or EI spacers.

The areas of source, drain and grid are in addition covered with a layer of a metal silicide, respectively referred DS 1, SS 1 and GS 1, in order to allow the contact of these areas with example the first level of metallization of the integrated circuit via metallized holes of interconnection commonly indicated by the specialist of the profession under the term of ' Farmhouse ".

This stage of realization, the whole of the conducting semi plate is covered with an insulating layer 2, typically out of silicon nitride. This insulating layer 2 itself is covered with a thicker layer of a dielectric material 3, for example of the silicon TEOS tétraorthosilicate. This last is typically deposited in a way in conformity, i.e. it marries the asperities of the integrated circuit.

The layer of the silicon nitride 2 and lays down it TEOS 3 form together an insulating layer which will separate the conducting semi substrate and the transistors, of the first level of metallization integrated circuit which will be carried out on the upper surface of layer 3 after flattening of the latter.

The various stages having allowed the integrated circuit realization until the deposit of layer 3, are traditional stages good known of the specialist of the profession, which are not described in detail ' ', and which are not the subject of this invention.

From the configuration illustrated on figure 1, the first stage of the process according to the invention consists in discovering the areas of grids G1, G101, of the transistors of the integrated circuit. For that, one withdraws the insulating layer covering the integrated circuit, i.e. one withdraws successively layers 3 and 2. This withdrawal is carried out by known traditional operations in themselves, and comprising for example a chemical mechanical polishing with possibly stop on the layer of silicon nitride, then a chemical engraving of this layer of silicon nitride. One also withdraws the layer of metal silicide GS 1, 101, in order to obtain the illustrated configuration figure 2. On this figure, reference 30 indicates the remainder of TEOS after setting with lines of polysilicon of the integrated circuit. It is advisable to note here that the initial presence of the layer of silicide of metal 1 and GS 101 is of no importance for the invention since it is withdrawn. Also, in certain cases, it is possible not to form this layer GS 1 and GS 101 on the grids of transistors T1 and T101 of figure 1. The setting with naked of the lines polysilicon will then comprise simply a withdrawal of layers 3 and 2. According to the invention, one proceeds then to a selective deposit of silicon, epitaxial type, not intentionally doped, on all the areas of polysilicon discovered, i.e. in the species on the areas of grids G1 and G101. Such a selective epitaxy can be carried out for example in a furnace by using a flow of dichlorosilane under a temperature ranging between 700 and 900

C approximately. The specialist of the profession will be able to adjust the pressure according to the temperature and of the desired degree of selectivity.

Because of the selective character of the epitaxy, the polysilicon grows only on the areas of grids G1 and G101, in order to form, like illustrated on figure 3, of the extensions of grids GX 1 and GX 101. In addition, according to thickness EP of polysilicon deposited, and because of the polycrystalline character of the silicon of the grids G1 and G101, the polysilicon deposited will be able to extend laterally at a distance DL proportional to thickness EP. Report/ratio EP/DL will depend on the conditions of the selective epitaxy. One can then obtain, according to thickness EP deposited, a grid resulting having the form from one T and made of a lower part G1 (the initial grid transistor) overcome of an extension of GXI grid overflowing laterally by report/ratio the lower part G L.

One then proceeds (figure 4) to a stage of silicidization of these extensions of grids in order to form, in this case the totality of the extensions of grids, of layers GXS 1 and GXS 101 of metal silicide. This stage of silicidization will consume a part of polysilicon of the extension of grids but without affecting the junctions source/substrate and drain/substrate transistors nor subjacent grid GX 1.

It is advisable to note here that, according to the invention, one can adjust thickness EP of polysilicon deposited as well as the thickness of the layer of metal silicide according to the value of the resistance desired for the final grid of the transistor.

In addition, this stage of silicidization can be done at low temperature (for example about 500 C This stage of silicidization is carried out by deposit of a metal, such as titanium, cobalt, nickel, tungsten, then, after the reaction of silicidization, one carries out a selective shrinking of metal not having reacted to leave metal silicide only on the extensions of grids GX1.

One thus obtains, into final, as illustrated on figure 5, a transistor T1 whose grid is made of a lower part G1 surrounded by insulating spacers E1 and of an extension of grid GX1 overcoming the lower part and covered at least partially with a layer of a metal silicide GXS 1.

In the example illustrated on figure 5, the extension of grid covered with the layer of metal silicide is broader than the lower part of the grid and the extension of grid is completely covered with the layer of metal silicide.

The continuation of the realization of the integrated circuit comprises for example a deposit in conformity of an oxide coating TEOS 31 on layer 30, in order to find itself in a configuration similar to that of figure 1. One could also deposit a doped dielectric material with the phosphorus possibly covered with a dielectric material un-doped, for example of the TEOS. One will then possibly procedure with a flattening of this layer 1, in order to be able to carry out on his upper surface the first level of metallization which will be then supplemented in a traditional way by higher levels of metallization, mutually inter-connected by vias. It is however advisable to note here that this flattening is not essential if the relief obtained is weak and compatible with the traditional later stages of manufacture of the integrated circuit.